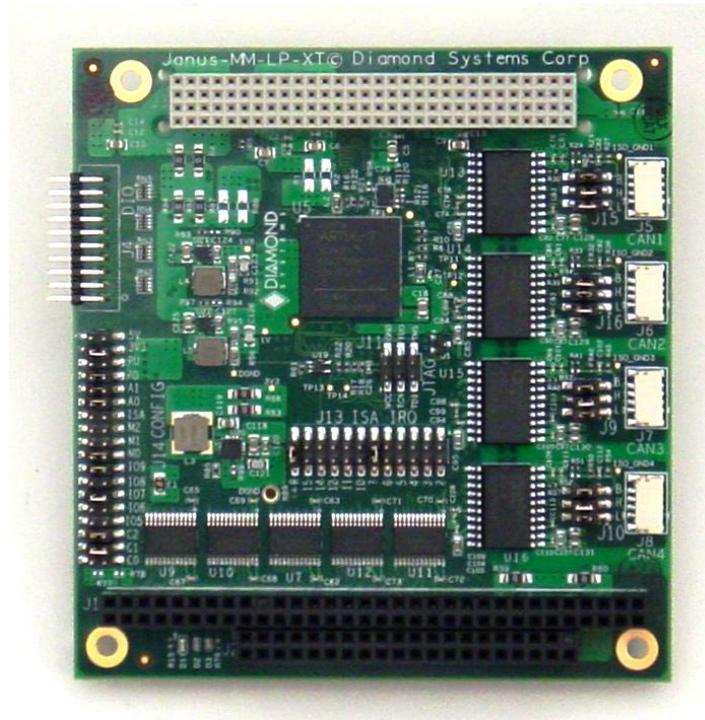




# Janus-MM-4LP User Manual

PC/104-Plus Dual or Quad CAN Port Module



Revision	Date	Comment
A.00	12/16/2015	Initial release

**FOR TECHNICAL SUPPORT  
PLEASE CONTACT:**

[support@diamondsystems.com](mailto:support@diamondsystems.com)

© Copyright 2015  
Diamond Systems Corporation  
555 Ellis Street  
Mountain View, CA 94043 USA  
Tel 1-650-810-2500  
Fax 1-650-810-2525  
[www.diamondsystems.com](http://www.diamondsystems.com)

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## 1. IMPORTANT SAFE HANDLING INFORMATION



### WARNING!

#### ESD-Sensitive Electronic Equipment

Observe ESD-safe handling procedures when working with this product.

Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.

Always store this product in ESD-protective packaging when not in use.

#### Safe Handling Precautions

This board contains a high density connector with many connections to sensitive electronic components. This creates many opportunities for accidental damage during handling, installation and connection to other equipment. The list here describes common causes of failure found on boards returned to Diamond Systems for repair. This information is provided as a source of advice to help you prevent damaging your Diamond (or any vendor's) embedded computer boards.

**ESD damage** – This type of damage is usually almost impossible to detect, because there is no visual sign of failure or damage. The symptom is that the board eventually simply stops working, because some component becomes defective. Usually the failure can be identified and the chip can be replaced. To prevent ESD damage, always follow proper ESD-prevention practices when handling computer boards.

**Damage during handling or storage** – On some boards we have noticed physical damage from mishandling. A common observation is that a screwdriver slipped while installing the board, causing a gouge in the PCB surface and cutting signal traces or damaging components.

Another common observation is damaged board corners, indicating the board was dropped. This may or may not cause damage to the circuitry, depending on what is near the corner. Most of our boards are designed with at least 25 mils clearance between the board edge and any component pad, and ground / power planes are at least 20 mils from the edge to avoid possible shorting from this type of damage. However these design rules are not sufficient to prevent damage in all situations.

A third cause of failure is when a metal screwdriver tip slips, or a screw drops onto the board while it is powered on, causing a short between a power pin and a signal pin on a component. This can cause overvoltage / power supply problems described below. To avoid this type of failure, only perform assembly operations when the system is powered off.

Sometimes boards are stored in racks with slots that grip the edge of the board. This is a common practice for board manufacturers. However our boards are generally very dense, and if the board has components very close to the board edge, they can be damaged or even knocked off the board when the board tilts back in the rack. Diamond recommends that all our boards be stored only in individual ESD-safe packaging. If multiple boards are stored together, they should be contained in bins with dividers between boards. Do not pile boards on top of each other or cram too many boards into a small location. This can cause damage to connector pins or fragile components.

**Power supply wired backwards** – Our power supplies and boards are not designed to withstand a reverse power supply connection. This will destroy each IC that is connected to the power supply (i.e. almost all ICs). In this case the board will most likely will be unrepairable and must be replaced. A chip destroyed by reverse power or by excessive power will often have a visible hole on the top or show some deformation on the top surface due to vaporization inside the package. **Check twice before applying power!**

**Overvoltage on digital I/O line** – If a digital I/O signal is connected to a voltage above the maximum specified voltage, the digital circuitry can be damaged. On most of our boards the acceptable range of voltages connected to digital I/O signals is 0-5V, and they can withstand about 0.5V beyond that (-0.5 to 5.5V) before being damaged. However logic signals at 12V and even 24V are common, and if one of these is connected to a 5V logic chip, the chip will be damaged, and the damage could even extend past that chip to others in the circuit

## 2. INTRODUCTION

### 2.1 Description

The Janus-MM-4LP-XT family of I/O modules offers two or four opto-isolated CANbus 2.0B ports plus 16 digital I/O lines. Models are available in both the PC/104-*Plus* and PC/104 form factors. Janus-MM-4LP is based on Xilinx Artix-7 FPGA. This core houses the CAN controller logic and digital I/O logic providing data rates up to 1Mbps. Each CAN port supports standard and extended frames as well as expanded TX and RX message queues for enhanced performance. Each port has its own combination isolator and transceiver chip. The 16 digital I/O lines have a selectable voltage level of +3.3V or +5V.

### 2.2 Features

- ◆ 2 or 4 CAN 2.0B compatible ports
- ◆ Data rates up to 1Mbps
- ◆ Supports standard 11-bit identifier and extended 29-bit identifier frames
- ◆ Extended TX and RX message queues for enhanced performance
- ◆ 16 8-byte transmit message queues
- ◆ 31 8-byte receive message queues
- ◆ 16 receive filters
- ◆ Galvanically isolated transceivers
- ◆ 500V port-to-host and port-to-port isolation
- ◆ Jumper selectable biased split termination for improved noise reduction
- ◆ 16 digital I/O lines
- ◆ Latching I/O connectors for increased ruggedness
- ◆ PCI and ISA bus interfaces

### 2.3 Operating System Support

Windows Embedded 7 and Linux Ubuntu 12.04LTS  
Basic CAN driver included with APIs and monitor program

### 2.4 Mechanical, Electrical, Environmental

- ◆ PC/104-*Plus* form factor compliant, 3.55" x 3.775" (90mm x 96mm) without wings
- ◆ -40°C to +85°C ambient operating temperature
- ◆ Power input requirements: +5VDC +/- 5%
- ◆ PCI (3.3V) and ISA (5V) host interfaces
- ◆ MIL-STD-202G shock and vibration compatible

### 3. FUNCTIONAL OVERVIEW

#### 3.1 Functional Block Diagram

Figure 1 shows the block diagram for Janus-MM-4LP.

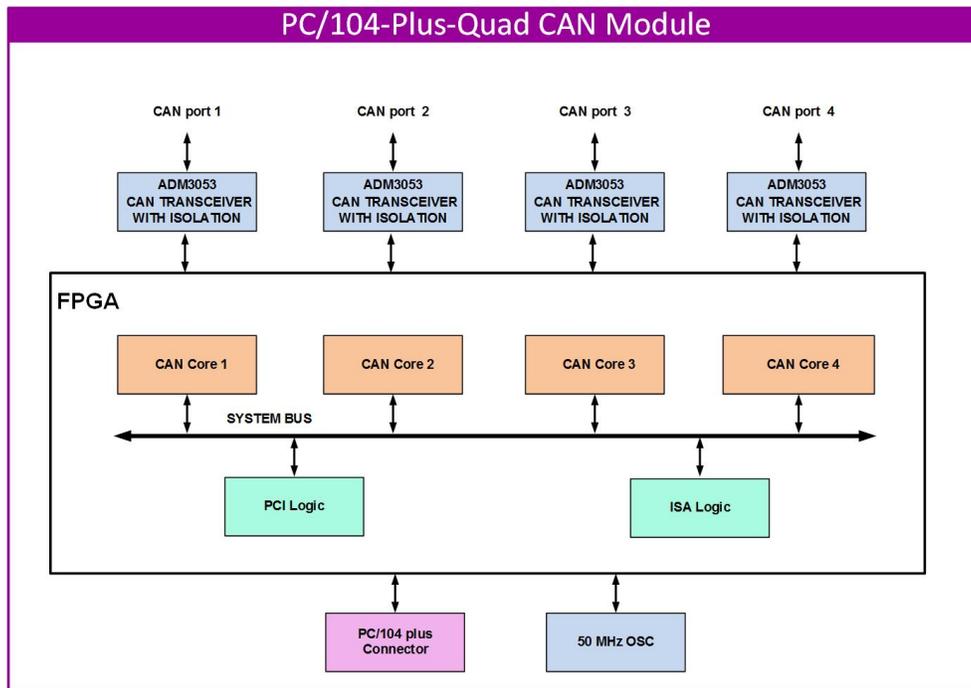


Figure 1: Block Diagram

### 3.2 Mechanical Board Drawing

Figure 2 shows the mechanical drawing for Janus-MM-4LP. The module adheres to the PC/104-Plus standard.

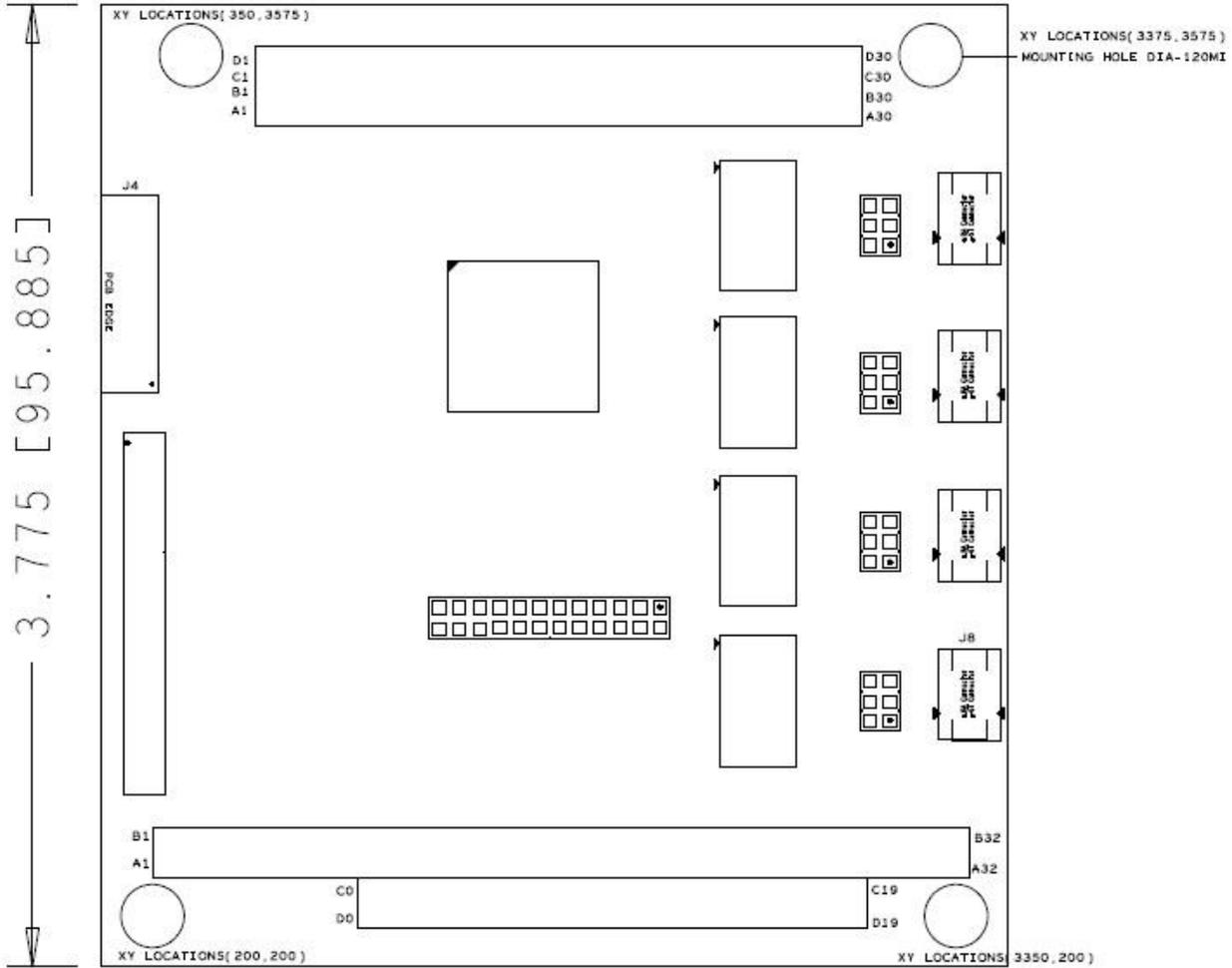


Figure 2: Mechanical Drawing

## 3.3 Key Subsystems

### 3.3.1 CAN Controllers

The module has two or four CANbus 2.0 controllers implemented as FPGA cores inside a Xilinx Artix-7 FPGA. The FPGA core provides the following key features:

- Conforms to the ISO 11898 -1, CAN 2.0A, and CAN 2.0B standards
- Supports both standard (11-bit identifier) and extended (29-bit identifier) frames
- Supports bit rates up to 1Mbps
- Transmit message FIFO with a user-configurable depth of up to 64 messages
- Transmit prioritization through one High-Priority Transmit buffer
- Automatic re-transmission on errors or arbitration loss
- Receive message FIFO with a user-configurable depth of up to 64 messages
- Acceptance filtering with a user-configurable number of up to 16 acceptance filters
- Sleep Mode with automatic wake-up
- Loop Back Mode for diagnostic applications
- Maskable Error and Status Interrupts
- Readable Error Counters

### 3.3.2 CAN Transceivers

The CAN transceivers are Analog Devices ADM3053 with a combination of isolation and transceiver. The device is powered by +5V. It generates isolated power to power the isolated side of the transceiver and the transceivers feature programmable slope control with a resistor.

### 3.3.3 Isolation

Janus-MM-4LP supports 500V isolation between each CAN port and the host, and between each CAN port and the other via the ADM3053 isolated transceiver. An insulating film has been added to the bottom of the PCB in the isolated area for additional protection.

### 3.3.4 Digital I/O

Janus-MM-4LP offers 16 digital I/O lines organized in two 8-bit I/O ports which are buffered with external data transceivers. The logic levels are jumper-selectable for 3.3V or 5V operation, and the DIO lines have jumper-selectable pull-up / pull-down resistors. The entire circuit is enabled or disabled based on the settings of 3 I/O configuration jumpers. When the circuit is enabled, the 8-bit ports are accessed at registers Base + 0 (Port A) and Base + 1 (Port B), where Base is the base address selected with jumpers JA9-5.

The ports power-up and reset to 0 and input mode. When a port is in output mode, its I/O pins are in output mode and reflect the value of the corresponding output registers, and these output values may also be read back during a read cycle to the port's address. When a port is in input mode, its I/O pins are in input mode, and their values are read back during a read cycle to the port's address.

Each port's direction is controlled by a bit in a control register at Base + 3. When a control bit is 0, the port is in input mode, and when it is 1, the port is in output mode. The control register powers up and resets to 0. The control register may also be read back during a read cycle to Base + 3.

The FPGA has an output pin P\_LED which can be used to drive an LED to indicate the FPGA is alive and responding to commands. P\_LED is controlled by the LED bit in the register at base + 2. The pin logic level is the opposite of the register value. On power-up or reset the register bit is 1 and the pin is low, turning the LED on. A 0 turns the LED off.

Offset	7	6	5	4	3	2	1	0
0 (R/W)	DIOA7	DIOA6	DIOA5	DIOA4	DIOA3	DIOA2	DIOA1	DIOA0
1 (R/W)	DIOB7	DIOB6	DIOB5	DIOB4	DIOB3	DIOB2	DIOB1	DIOB0
2 (W)								LED
2 (R)								
3 (R/W)							DIRB	DIRA

### 3.3.5 Power Supply

The module is powered by +5V from the PCI and ISA connectors. It provides all other required voltages on board, including +3.3V for the CAN transceivers and the FPGA core voltages.

The digital I/O connector provides power for external circuitry. The voltage is selected between 3.3V and 5V with a jumper which also controls the voltage of the digital I/O transceivers. The current is limited via a poly-switch thermal resettable fuse with a hold current capacity of 350mA.

### 3.3.6 Multi Host Interface

The FPGA used on the board contains a PCI interface core and ISA interface core. Both the PCI and ISA interfaces are available. Only one bus interface can be active at any time. The active interface is selected with a bus power (+5V) signal from the PCI connector routed through a jumper to an input pin on the FPGA. If the FPGA detects a high on the input pin, the PCI interface is used; otherwise the ISA interface is used.

If the PCI interface is not selected, it is inactive, and all FPGA PCI interface pins are tristated. Likewise, if the ISA interface is not selected, it is inactive, and all FPGA ISA bus interface pins are tristated.

### 3.3.7 PCI Bus Interface

The FPGA includes a 32-bit 33MHz PCI core that interfaces to the PC/104-*Plus* PCI. The PCI host interface may be selected by a combination of power pin detection and jumper enable. The PCI interface includes 5 memory address ranges: four for the CAN controllers and one for the general purpose.

The PCI interface is active when the FPGA detects the presence of the PCI bus and a jumper option is selected. Presence is detected by one +5V pin from the PCI connector connected to an input pin P\_PCISEL on the FPGA via a jumper. This FPGA pin has a pull-down resistor connected to it. If the pin is high, the PCI bus is selected; otherwise the ISA interface is selected.

The PCI interface uses 3.3V logic levels. No level translators are required to interface the FPGA to the PCI-104 bus. The PCI-104 connector must be labeled as a 3.3V only interface, since it is not 5V tolerant.

### 3.3.8 PCI Configuration Space

The PCI configuration space requires the use of five base address registers or BARs with the following parameters:

BAR Number	Function	Type	Size
0	CAN1	Memory	As required by CAN core
1	CAN2	Memory	As required by CAN core
2	CAN3	Memory	As required by CAN core
3	CAN4	Memory	As required by CAN core
4	I/O block	Memory	32 bytes (only the first 4 are currently used)

The PCI configuration space has the following ID information:

Vendor ID:     **0x4453**  
 Device ID:     **0x1100**

### 3.3.9 ISA host Interface

The FPGA includes an ISA host interface with 16-bit I/O addressing, 24-bit memory addressing, and 8-bit data. The interface is compatible with PC/104 implementations on embedded computers. It uses IRQ but no DMA. The ISA interface is 5V compliant. External level shifting transceivers are used between the FPGA and the PC/104 connector to provide this compatibility. All transceivers are one way except the data bus transceiver which is bidirectional. The direction of this bidirectional transceiver is controlled with the FPGA signal P\_RD. When P\_RD is low, the data direction is from the ISA connector to the FPGA (ISA write cycle addressing one of the active I/O windows or idle), and when it is high the direction is from the FPGA to the ISA bus (ISA read cycle addressing one of the active I/O windows).

The ISA interface offers two memory address ranges for the CAN controllers and one I/O address range for the digital I/O interface described below.

## 4. BOARD LAYOUT

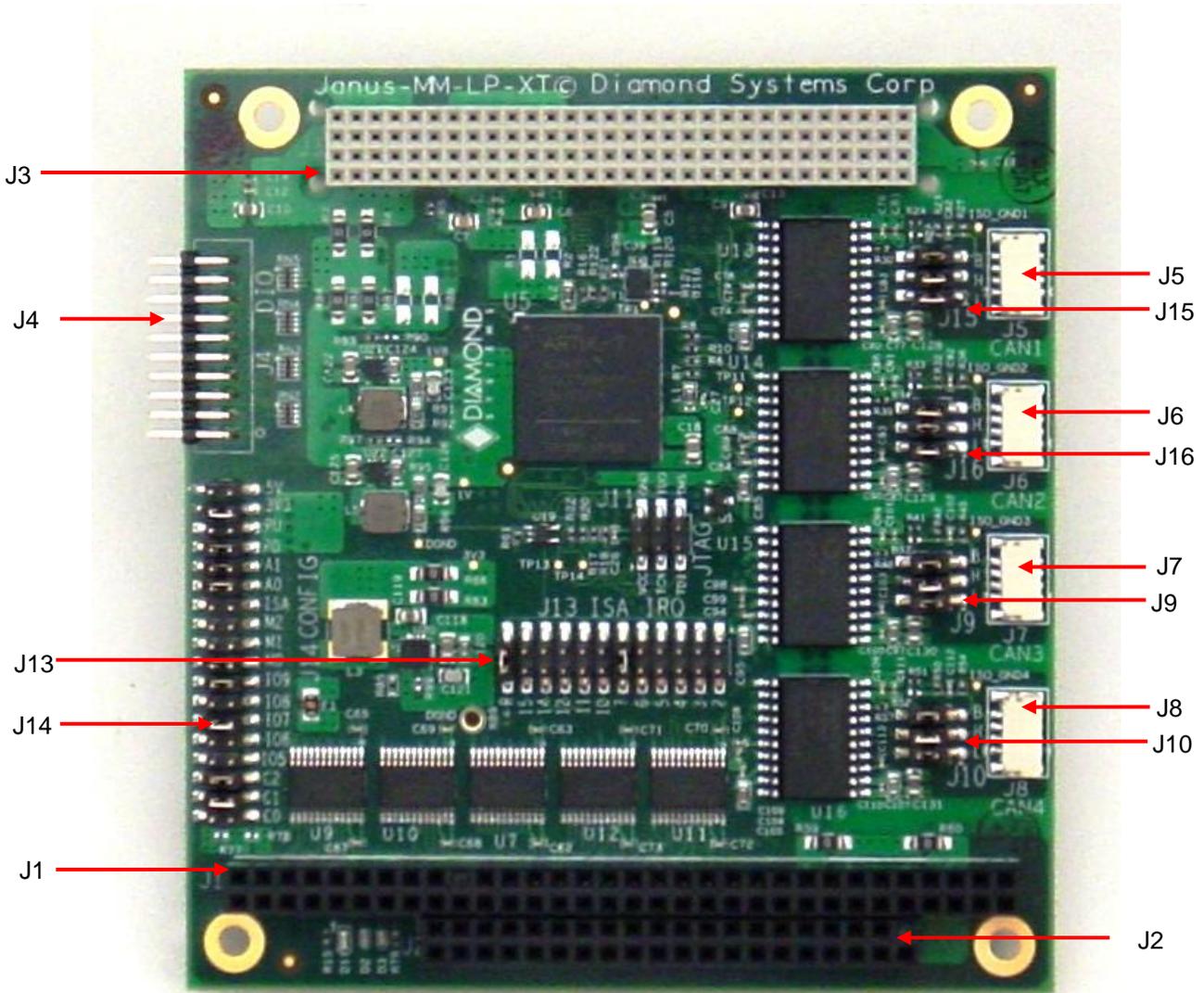


Figure 3: JNMM-4LP Board Layout

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## 4.1 Connector and Jumper List

<b>Connector</b>	<b>Description</b>
J1	PC/104 bus 8-bit ISA connector
J2	PC/104 bus 16-bit ISA connector
J3	PC/104-Plus PCI connector
J4	Digital I/O connector
J5	CAN1 connector
J6	CAN2 connector
J7	CAN3 connector
J8	CAN4 connector
J9	Termination jumper block for CAN3
J10	Termination jumper block for CAN4
J13	ISA IRQ jumper block
J14	Configuration jumper block
J15	Termination jumper block for CAN1
J16	Termination jumper block for CAN2

## 5. CONNECTOR PINOUT AND PIN DESCRIPTION

### 5.1 CAN (J5, J6, J7, J8)

Each of the four CAN ports has its own 4-pin latching connector with the same pinout as shown below. These connectors are located on the right side of the board. CAN1 (J5) is the topmost connector and CAN4 (J8) is the bottommost connector.

1	Ground Iso
2	CAN L
3	CAN H
4	Ground Iso

#### Connector Part Number / Description

JST SM04B-GHS-TB 4 pos, 1.25mm, right angle, latching, SMD

### 5.2 Digital I/O (J4)

The sixteen digital I/O lines are brought out on a 20-pin pin header, J4, with the pinout shown below.

<b>J4</b>		
DIO A0	<b>1</b>	<b>2</b> DIO A1
DIO A2	<b>3</b>	<b>4</b> DIO A3
DIO A4	<b>5</b>	<b>6</b> DIO A5
DIO A6	<b>7</b>	<b>8</b> DIO A7
DIO B0	<b>9</b>	<b>10</b> DIO B1
DIO B2	<b>11</b>	<b>12</b> DIO B3
DIO B4	<b>13</b>	<b>14</b> DIO B5
DIO B6	<b>15</b>	<b>16</b> DIO B7
V fused	<b>17</b>	<b>18</b> V fused
Ground	<b>19</b>	<b>20</b> Ground

#### Connector Part Number / Description

OUPIN 2112-2210G00R 2mm pitch dual row right angle pin header with ejector latches

### 5.3 ISA Connector (J1 & J2)

The board contains the non-stack-through / short pin 8-bit and 16-bit PC/104 connectors on the top side in the standard position as described by the PC/104-Plus specification.

#### J2: PC/104 16-bit bus connector

Ground	<b>D0</b>	<b>C0</b>	Ground
MEMCS16-	<b>D1</b>	<b>C1</b>	SBHE-
IOCS16-	<b>D2</b>	<b>C2</b>	LA23
IRQ10	<b>D3</b>	<b>C3</b>	LA22
IRQ11	<b>D4</b>	<b>C4</b>	LA21
IRQ12	<b>D5</b>	<b>C5</b>	LA20
IRQ15	<b>D6</b>	<b>C6</b>	LA19
IRQ14	<b>D7</b>	<b>C7</b>	LA18
DACK0-	<b>D8</b>	<b>C8</b>	LA17
DRQ0	<b>D9</b>	<b>C9</b>	MEMR-
DACK5-	<b>D10</b>	<b>C10</b>	MEMW-
DRQ5	<b>D11</b>	<b>C11</b>	SD8
DACK6-	<b>D12</b>	<b>C12</b>	SD9
DRQ6	<b>D13</b>	<b>C13</b>	SD10
DACK7-	<b>D14</b>	<b>C14</b>	SD11
DRQ7	<b>D15</b>	<b>C15</b>	SD12
+5V	<b>D16</b>	<b>C16</b>	SD13
MASTER-	<b>D17</b>	<b>C17</b>	SD14
Ground	<b>D18</b>	<b>C18</b>	SD15
Ground	<b>D19</b>	<b>C19</b>	Key

#### J1: PC/104 8-bit bus connector

IOCHCHK-	<b>A1</b>	<b>B1</b>	Ground
SD7	<b>A2</b>	<b>B2</b>	RESET
SD6	<b>A3</b>	<b>B3</b>	+5V
SD5	<b>A4</b>	<b>B4</b>	IRQ9
SD4	<b>A5</b>	<b>B5</b>	-5V
SD3	<b>A6</b>	<b>B6</b>	DRQ2
SD2	<b>A7</b>	<b>B7</b>	-12V
SD1	<b>A8</b>	<b>B8</b>	0WS-
SD0	<b>A9</b>	<b>B9</b>	+12V
IOCHRDY	<b>A10</b>	<b>B10</b>	Key
AEN	<b>A11</b>	<b>B11</b>	SMEMW-
SA19	<b>A12</b>	<b>B12</b>	SMEMR-
SA18	<b>A13</b>	<b>B13</b>	IOW-
SA17	<b>A14</b>	<b>B14</b>	IOR-
SA16	<b>A15</b>	<b>B15</b>	DACK3-
SA15	<b>A16</b>	<b>B16</b>	DRQ3
SA14	<b>A17</b>	<b>B17</b>	DACK1-
SA13	<b>A18</b>	<b>B18</b>	DRQ1
SA12	<b>A19</b>	<b>B19</b>	Refresh-
SA11	<b>A20</b>	<b>B20</b>	SYSCLK
SA10	<b>A21</b>	<b>B21</b>	IRQ7
SA9	<b>A22</b>	<b>B22</b>	IRQ6
SA8	<b>A23</b>	<b>B23</b>	IRQ5
SA7	<b>A24</b>	<b>B24</b>	IRQ4
SA6	<b>A25</b>	<b>B25</b>	IRQ3
SA5	<b>A26</b>	<b>B26</b>	DACK2-
SA4	<b>A27</b>	<b>B27</b>	TC
SA3	<b>A28</b>	<b>B28</b>	BALE
SA2	<b>A29</b>	<b>B29</b>	+5V
SA1	<b>A30</b>	<b>B30</b>	OSC
SA0	<b>A31</b>	<b>B31</b>	Ground
Ground	<b>A32</b>	<b>B32</b>	Ground

#### Connector Part Number / Description

- J1: EPT Connectors 962-60323-12 64 pins .435" high solder tails  
 J2: EPT Connectors 962-60203-12 40 pins .435" high solder tails

## 5.4 PC-104 (J3)

The board contains a non-stack through / short pin PC-104 connector, J3, on the top side in the standard position as described by the PC/104-Plus specification.

J3				
Pin	A	B	C	D
1	GND/5.0V KEY <sup>2</sup>	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	Reserved	Reserved	GND/3.3V KEY <sup>2</sup>

**Connector Type:** 30 x 4 pin 2mm pitch with solder tails

## 6. JUMPER CONFIGURATION

The module provides the following jumper configurations. All jumpers are implemented in 2mm pitch jumper blocks. The following functionality can be selected by jumpers.

- PCI or ISA bus interface
- PCI slot selection
- CAN circuit memory base addresses in ISA mode
- DIO circuit I/O base address in ISA mode
- VIO +3.3V / +5V selection for digital I/O lines and power output on digital I/O connector
- ISA IRQ level and IRQ pulldown resistor configuration
- 120-ohm line termination and bias resistors for each CAN port

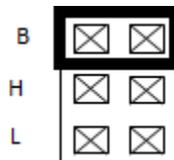
Each CAN port has its own jumper block for biased split termination. The ISA IRQ settings are contained on one jumper block. All the other jumper options are combined into a single jumper block. All jumper positions are labeled on the board for easy user comprehension.

Optionally, 0 ohm resistors can be used instead of jumpers for rugged applications where jumpers are not desired. Contact Diamond Systems for more information.

### 6.1 Termination Jumpers (J9, J10, J15, J16)

The Janus-MM-4LP module has four biased split termination jumper blocks, one for each CAN port. Jumper block J15 is for CAN1 (J5), jumper block J16 is for CAN2 (J7), jumper block J9 for CAN3 (J7) and jumper block J10 for CAN4 (J8). Jumper blocks J15, J16, J9 and J10 are identical. The default is jumpers installed in all three positions; B, H and L. To add termination for a port's bias line, CAN-H line, or CAN-L line, add a jumper at the B, H or L location respectively.

Figure 4 illustrates adding a jumper for a port's bias line only.



**Figure 4: Termination Jumper Block**

## 6.2 ISA IRQ Jumper (J13)

Jumper block J13 is used to change the status of the IRQ signals. One side of the jumper is connected to the IRQ signal, the other side is connected to the pull-up or pull-down option which is selected by the jumper R and controlled by the FPGA. All 5V/GND pins are shorted and connected to a 5V supply which is enabled by R. The default is jumpers installed on positions IRQ7 and R which enables the pull-down resistors.

J13			Jumper Information
<input type="radio"/>	<input type="radio"/>	IRQ2	
<input type="radio"/>	<input type="radio"/>	IRQ3	
<input type="radio"/>	<input type="radio"/>	IRQ4	
<input type="radio"/>	<input type="radio"/>	IRQ5	
<input type="radio"/>	<input type="radio"/>	IRQ6	
<input checked="" type="radio"/>	<input checked="" type="radio"/>	IRQ7	Jumper installed default
<input type="radio"/>	<input type="radio"/>	IRQ10	
<input type="radio"/>	<input type="radio"/>	IRQ11	
<input type="radio"/>	<input type="radio"/>	IRQ12	
<input type="radio"/>	<input type="radio"/>	IRQ14	
<input type="radio"/>	<input type="radio"/>	IRQ15	
<input checked="" type="radio"/>	<input checked="" type="radio"/>	R	Jumper installed default

### 6.3 Configuration Jumper (J14)

Jumper block J14 has the following configuration options:

J14			Functional Description	Jumper Information
<input type="radio"/>	<input type="radio"/>	5V	+5V digital I/O logic level	One of 5V or 3V3 must be selected
<input type="radio"/>	<input type="radio"/>	3V3	+3.3V digital I/O logic level	One of 5V or 3V3 must be selected (default)
<input type="radio"/>	<input type="radio"/>	PU	Digital I/O lines pull-up	One of PU or PD must be selected
<input type="radio"/>	<input type="radio"/>	PD	Digital I/O lines pull-down	One of PU or PD must be selected (default)
<input type="radio"/>	<input type="radio"/>	A1	PCI slot select A1	See PCI Slot Select Table (default)
<input type="radio"/>	<input type="radio"/>	A0	PCI slot select A0	(default)
<input type="radio"/>	<input type="radio"/>	PCI	ISA / PCI select	Install jumper for ISA
<input type="radio"/>	<input type="radio"/>	M2	CAN base address M2	See CAN Base Address Table
<input type="radio"/>	<input type="radio"/>	M1	CAN base address M1	
<input type="radio"/>	<input type="radio"/>	M0	CAN base address M0	(default)
<input type="radio"/>	<input type="radio"/>	IO9	DIO base address IO9	See DIO Base Address Table (default)
<input type="radio"/>	<input type="radio"/>	IO8	DIO base address IO8	
<input type="radio"/>	<input type="radio"/>	IO7	DIO base address IO7	(default)
<input type="radio"/>	<input type="radio"/>	IO6	DIO base address IO6	
<input type="radio"/>	<input type="radio"/>	IO5	DIO base address IO5	
<input type="radio"/>	<input type="radio"/>	C2	Factory use only	(default)
<input type="radio"/>	<input type="radio"/>	C1	Factory use only	(default)
<input type="radio"/>	<input type="radio"/>	C0	Factory use only	

PCI Slot Select Table:

A0	A1	PCI Slot #
0	0	00
1	0	10
0	1	01
1	1	11 (default)

CAN Base Address Table:

M2	M1	M0	Base Address	CAN0	CAN1	CAN2	CAN3
0	0	0	0xE000	0xE000 to 0xE0FF	0xE100 to 0xE1FF	0xE200 to 0xE2FF	0xE300 to 0xE3FF
0	0	1	0x1000 (default)	0x1000 to 0x10FF	0x1100 to 0x11FF	0x1200 to 0x12FF	0x1300 to 0x13FF
0	1	0	0x2000	0x2000 to 0x20FF	0x2100 to 0x21FF	0x2200 to 0x22FF	0x2300 to 0x23FF
0	1	1	0x3000	0x3000 to 0x30FF	0x3100 to 0x31FF	0x3200 to 0x32FF	0x3300 to 0x33FF
1	0	0	0x4000	0x4000 to 0x40FF	0x4100 to 0x41FF	0x4200 to 0x42FF	0x4300 to 0x43FF
1	0	1	0x5000	0x5000 to 0x50FF	0x5100 to 0x51FF	0x5200 to 0x52FF	0x5300 to 0x53FF
1	1	0	0x6000	0x6000 to 0x60FF	0x6100 to 0x61FF	0x6200 to 0x62FF	0x6300 to 0x63FF
1	1	1	0x7000	0x7000 to 0x70FF	0x7100 to 0x71FF	0x7200 to 0x72FF	0x7300 to 0x73FF

Digital I/O Base Address Table:

IO9	IO8	IO7	IO6	IO5	Base Address
0	1	0	0	X	0x0100
0	1	0	1	X	0x0140
0	1	1	0	X	0x0180
0	1	1	1	X	0x01C0
1	0	0	0	X	0x0200
1	0	0	1	X	0x0240
1	0	1	0	X	0x0280 (default)
1	1	0	1	X	0x0340

## 7. SPECIFICATIONS

<b>General</b>	
Number of ports	2 or 4 CAN 2.0B ports
Data rate	1Mbps
Controller	FPGA based
Transceiver	ADM3053 isolation + transceiver
Isolation	500V port-to-host and port-to-port
Frames	Standard 11-bit identifier Extended 29-bit identifier
Message queues	Expanded TX and RX message queues 16 8-byte transmit message queues 31 8-byte receive message queues
Receive filters	16
Termination	Jumper selectable biased split termination
Digital I/O	16 programmable digital I/O lines arranged in 2 8-bit ports
Logic levels	3.3V or 5V, jumper selectable
Pull-up / pull-down	Jumper selectable
Direction control	Software programmable
Host interface	PCI or ISA, self selecting
OS support	Windows Embedded 7 and Linux Ubuntu 12.04LTS APIs and monitor programs included
<b>Mechanical / Environmental</b>	
Input power	+5VDC +/-5%
Power consumption	W at 5VDC
Operating temperature	-40°C to +85°C (-40°F to +185°F)
Operating humidity	5% to 95% non-condensing
Shock	MIL-STD-202G compatible
Vibration	MIL-STD-202G compatible
MTBF	Tbd hours at 20°C
Dimensions	3.55" x 3.775" (90mm x 96mm)
Weight	2.5oz (71g)
RoHS	Compliant